AMENDMENTS TO THE SPECIFICATION

Page 1, before paragraph 1, insert

This application is a divisional of U.S. serial no. 09/438,295, filed November 12, 1999, which is a divisional of U.S. serial no. 08/931,519, filed September 16, 1997.

Please replace page 1, paragraph 4 with the following amended paragraph:

Recently, however as disclosed by Japanese Laid-Open Patent No. [6(1994)-195687] 6(1994)-195987, there has been developed a multilevel semiconductor memory device which can store three or more levels of data each in a single memory cell. A plurality of threshold voltages are set in the multilevel semiconductor memory device. For instance, in the case of four-level non-volatile semiconductor memory, four threshold voltages (OV, 2V, 4V, 6V) are set to each memory cell, respectively, so that two-bit data can be stored in a single memory cell. In other words, the threshold voltage of the memory cell is set to any one of OV, 2V, 4V and 6V in correspondence to each of four storage contents of (00, 01, 10, 11).

Please replace page 5, paragraph 2 with the following amended paragraph:

As described above, in the multilevel semiconductor memory device, data are output after the data stored in the memory cell has been perfectly specified in the read operation, irrespective of the input logical address. There exists a problem in that a time longer than [necessity] necessary is needed, with the result that the data reading speed is inevitably limited.

Please replace pages 8-9, paragraph 2 with the following amended paragraph:

Further, the present invention provides a computer readable medium storing program code f or causing a computer to read n ($n \geq 2$) number of bits (x1, x2, ..., xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell storing 2^n levels of data each expressed by the bits (xl, x2, ..., xn), comprising: first program code means for converting a logical address into a physical address included in the physical address

space; second program code means [fop] for judging whether a logical address space including the logical address matches the physical address space; third program code means for specifying the most significant bit xl, by one-time specifying operation, by means of a reference value when judged that the logical address space matches the physical address space; and fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

Please replace pages 13-14, paragraph 4 with the following amended paragraph:

Fig. 1 is a block diagram showing a main configuration of an EEPROM in the preferred embodiments according to the [p resent] present invention;

Please replace page 42, paragraph 1 with the following amended paragraph:

Therefore, when the data of the highest-order bit is read, it is possible to increase the access speed three times [hither] higher than that of when the respective threshold voltages are checked by use of all the reference voltages. Further, when the data of the medium-order bit is read, it is possible to increase the access speed about 1.5 times higher than that of when the respective threshold voltages are checked by use of all the decision voltages. Therefore, the data having the highest access frequency can be stored in the highest-order bits, the data having the medium access frequency in the medium-order bits, and the data having a relatively low access frequency in the lowest-order bits. A programmer thus can operate the EEPROM as if a single- or double-stage high speed memory devices were provided. It is thus possible to read data from the multilevel EEPROM in an extremely high efficiency.